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[Regression Models for Behavioral Power Estimation - group of 2 »](#) [All articles](#) [Recent articles](#)

L BENINI - Integrated Computer-Aided Engineering, 1998 - IOS Press

... Just one **RTL** simulation was required to obtain the ... context but it is not applicable to static **power estimation**. ... Assume that the **circuit** is **stable** at time  $t_1$  ...

[Cited by 42](#) - [Web Search](#) - [BL Direct](#)

[Node sampling: a robust RTL power modeling approach - group of 8 »](#)

A Bogliolo, L Benini - Computer-Aided Design, 1998. ICCAD 98. Digest of Technical ..., 1998 - [ieeexplore.ieee.org](#)

... assume  $T = 1$  and  $l'drl = 1$ , thus energy and **power** have ... not an **RTL** model for e.

We observe, however ... its mean value e, thus solving the energy **estimation** problem ...

[Cited by 14](#) - [Web Search](#)

[An effective power management scheme for RTL design based on multiple clocks - group of 5 »](#)

C Papachristou, M Spinning, M Nourani - Design Automation Conference Proceedings 1996, 33rd, 1996 - [ieeexplore.ieee.org](#)

... the effect of switching activities in our **power estimation**. ... difference between **Circuit 1** and **Circuit 2** i ... CLK3, 3.2 Timing Relationships and **Power** Consider two ...

[Cited by 17](#) - [Web Search](#) - [BL Direct](#)

[A multiple clocking scheme for low-power RTL design - group of 8 »](#)

CA Papachristou, M Nourani, M Spining - Very Large Scale Integration (VLSI) Systems, IEEE ..., 1999 - [ieeexplore.ieee.org](#)

... and frequency, we synthesize a group of **RTL circuit** structures implementing ... nonoverlapping clocks, respectively, and then **estimate** the **power** of each **RTL** ...

[Cited by 21](#) - [Web Search](#) - [BL Direct](#)

[Power management techniques for control-flow intensive designs - group of 10 »](#)

A Raghunathan, S Dey, NK Jha, K Wakabayashi - Proc. Design Automation Conf, 1997 - [doi.ieeecomputersociety.org](#)

... **Power**:  $S_0 S_1 S_2 S_3 S_4 S_5 \text{ tempX} + dX$  ... (b) (c) (a) Figure 1: (a) **RTL circuit** implementing the ... during which the controller makes the state **transition**  $S_2 \rightarrow S_3$ . ...

[Cited by 14](#) - [Web Search](#) - [BL Direct](#)

[Extracting RTL Models from Transistor Netlists - group of 8 »](#)

KJ Singh, PA Subrahmanyam - Proceedings of the 1995 IEEE/ACM international conference on ..., 1995 - [doi.ieeecomputersociety.org](#)

... not concerned with modeling the transient behavior in the **RTL** model (we assumed that the **circuit** has time ... 3(c) where there is a direct **transition** from one ...

[Cited by 15](#) - [Web Search](#) - [BL Direct](#)

[RTL level preparation of high-quality/low-energy/low-power BIST - group of 5 »](#)

MB Santos, IC Teixeira, JP Teixeira, S Manich, R ... - Test Conference, 2002. Proceedings. International, 2002 - [ieeexplore.ieee.org](#)

... a metric that is extensively used to **estimate** energy and ...  $E_0$  be the energy consumed by the **circuit** during the ... Mask Influence on Energy / **Power** Consumption The ...

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circuit power transition gate | RTL estimation

1970

- 2000

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A survey of power estimation techniques in VLSI circuits - group of 6 » [All articles](#) [Recent articles](#)

FN Najm - Very Large Scale Integration (VLSI) Systems, IEEE ..., 1994 - [ieeexplore.ieee.org](#)  
 ... current drawn by a logic gate, so that the short-circuit current during ... triggers  
 the latches, some of them will make a transition and will draw power. ...  
 Cited by 330 - [Web Search](#)

Power modeling for high-level power estimation - group of 20 »

S Gupta, FN Najm - Very Large Scale Integration (VLSI) Systems, IEEE ..., 2000 - [ieeexplore.ieee.org](#)  
 ... for an input combinational circuit is 2 ... transitions into clusters of input  
 transitions that have the ... to estimate switching activity and power consumption at ...  
 Cited by 134 - [Web Search](#) - [Library Search](#) - [BL Direct](#)

Estimation of average switching activity in combinational and sequential circuits - group of 3 »

A Ghosh, S Devadas, K Keutzer, J White - Proceedings of the 29th ACM/IEEE conference on Design ..., 1992 - [portal.acm.org](#)  
 ... the Boolean conditions that cause glitching (multiple transitions at a gate) in  
 the circuit. ... a significant percentage of the dissipated power or switching ...  
 Cited by 267 - [Web Search](#)

Register-transfer level estimation techniques for switching activity and power consumption - group of 15 »

A Raghunathan, S Dey, NK Jha - Proceedings of the 1996 IEEE/ACM international conference on ..., 1997 - [portal.acm.org](#)  
 ... 0 transition as half a transition, leading to ... running CSIM on the entire gate-level  
 circuit. ... RTL power estimation methodology The flowchart shown in Figure 2 ...  
 Cited by 73 - [Web Search](#) - [BL Direct](#)

Short-circuit power dissipation estimation for CMOS logic gates - group of 2 »

SR Vemuru, N Scheinberg - Circuits and Systems I: Fundamental Theory and Applications, ..., 1994 - [ieeexplore.ieee.org](#)  
 ... ratios of S and for gate lengths of ... Short-circuit power dissipation of CMOS inverter  
 obtained from ... simulations for various input transition times, capacitive ...  
 Cited by 41 - [Web Search](#)

A Monte Carlo approach for power estimation - group of 6 »

R Burch, FN Najm, P Yang, TN Trick, TI Inc, TX ... - Very Large Scale Integration (VLSI) Systems, IEEE ..., 1993 - [ieeexplore.ieee.org](#)  
 ... T) be the number of transitions of x ...  $s V_{dd} C_i$  —, where C<sub>i</sub> is the total capacitance  
 at i. The total average power dissipated in the circuit during the ...  
 Cited by 185 - [Web Search](#)

Towards a high-level power estimation capability [digital ICs] - group of 4 »

M Nemani, FN Najm - Computer-Aided Design of Integrated Circuits and Systems, ..., 1996 - [ieeexplore.ieee.org](#)  
 ... V is the average node transition density, defined ... then a viable high-level power  
 estimation methodology would ... simulation of the sequential circuit to measure ...  
 Cited by 79 - [Web Search](#) - [BL Direct](#)



toggle circuit power transition gate | RTL esti 1970 - 2000

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A survey of **power estimation** techniques in VLSI circuits - group of 6 » [All articles](#) [Recent articles](#)

FN Najm - Very Large Scale Integration (VLSI) Systems, IEEE ..., 1994 - [ieeexplore.ieee.org](#)  
... inputs are propagated into the **circuit** assuming spatial independence and the **power** was computed ... zero-delay model was used, the **toggle power** was ignored ...  
[Cited by 330](#) - [Web Search](#)

Feedback, correlation, and delay concerns in the **power estimation** of VLSI circuits - group of 10 »

FN Najm - Proceedings of the 32nd ACM/IEEE conference on Design ..., 1995 - [portal.acm.org](#)  
... Computing the **toggle power** is one main challenge in **power esti** ... How exactly do the **circuit** delays affect the ... is the activity (and, therefore, the **power**) to the ...  
[Cited by 19](#) - [Web Search](#) - [BL Direct](#)

Gate sizing for constrained delay/**power**/area optimization - group of 4 »

O Coudert - Very Large Scale Integration (VLSI) Systems, IEEE ..., 1997 - [ieeexplore.ieee.org](#)  
... **power estimation**. The **toggle rate** depends on how the signals propagate in the **circuit**. In particular, resizing a **gate** affects the glitches, ie, the **transitions** ...  
[Cited by 35](#) - [Web Search](#) - [BL Direct](#)

Application of **Toggle-Based Power Estimation** to Module Characterization

G Jochens, L Kruse, W Nebel - Proceedings of PATMOS (Power and Timing Modeling of ..., 1997 - [dice.ucl.ac.be](#)  
... switches is read from the **toggle count** output file, wire capacitances are ... cuits with a moderate **circuit-depth** an average error of about ... In this model the **power** ...  
[Cited by 5](#) - [View as HTML](#) - [Web Search](#)

Accurate logic-level **power estimation**

A Bogliolo, B Ricco, L Benini, G De Micheli - Low Power Electronics, 1995., IEEE Symposium on, 1995 - [ieeexplore.ieee.org](#)  
... observing the switch- ing actstnty (**toggle count**) at the ... spurious tran- sitions (glitches), short **circuit** currents and ... impact on the to- tal **power** dissipation. ...  
[Cited by 6](#) - [Web Search](#)

**Power estimation** of cell-based CMOS circuits - group of 5 »

A Bogliolo, L Benini, B Ricco - Proceedings of the 33rd annual conference on Design ..., 1996 - [portal.acm.org](#)  
... by looking at the switching activity (**toggle count**) and the ... parasitic phenomena (such as short-**circuit** currents, charging ... impact on the global **power**, cannot be ...  
[Cited by 16](#) - [Web Search](#) - [BL Direct](#)

**Power compiler: a gate-level power optimization and synthesis system** - group of 5 »

I Nedelchev - Proceedings of the 1997 International Conference on Computer ..., 1997 - [doi.ieeecomputersociety.org](#)  
... The definition of internal and short-**circuit power** in section ... The internal **power** model is a nonlinear model based on ... is then multiplied by the **toggle rate** of ...  
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Effects of delay models on peak **power estimation** of VLSI sequential circuits - group of 12 »


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 Coburn, J.; Ravi, S.; Raghunathan, A.;  
Design Automation Conference, 2005. Proceedings. 42nd  
 13-17 June 2005 Page(s):700 - 705  
[Abstract](#) | [Full Text: PDF\(483 KB\)](#) [IEEE CNF](#)  
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- ☐ **2. Hardware accelerated power estimation**  
 Coburn, J.; Ravi, S.; Raghunathan, A.;  
Design, Automation and Test in Europe, 2005. Proceedings  
 2005 Page(s):528 - 529 Vol. 1  
 Digital Object Identifier 10.1109/DATE.2005.168  
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